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A Novel Lateral Phase-Change Random Access Memory Characterized by Ultra Low RESET Current and Power Consumption

You YIN*, Akihira MIYACHI, Daisuke NIIDA, Hayato SONE and Sumio HOSAKA

Department of Nano-Material Systems, Graduate School of Engineering, Gunma University, 1-5-1 Tenjin, Kiryu, Gunma 376-8515, Japan

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We have fabricated and studied single lateral phase-change random-access-memory (PRAM), which has a confined $Ge_2Sb_2Te_5$ (GST) channel connected by two wide TiN electrodes of relatively low resistivity. Its switching current for RESET operation could be as low as 4–20 μA, about one or two orders of magnitude lower than that of the conventional bottom contact PRAM cell. Its corresponding switching power for RESET operation is about 2–4 μW. The reason for such ultra low RESET current and power could be that Joule heating occurred mainly in the GST channel, instead of the resistive heater in the conventional PRAM cell. [DOI: 10.1143/JJAP.45.L726]

KEYWORDS: phase change, chalcogenide, ultra low RESET current, ultra low power consumption, lateral PRAM

There is growing demand for nonvolatile memories characterized by fast write speed and high endurance with the rapid development of information society. As the mainstream in nonvolatile memory market today, flash memory, however, has many demerits such as long write/erase time, low endurance, high programming energy, high voltage, and limited scalability by tunnel oxide.[1] Electronic phase-change random-access memory (PRAM) is very promising as a candidate for next-generation nonvolatile memory. The principle of PRAM is on the basis of the ability of chalcogenides to be reversibly structure transformed between the highly resistive amorphous and lowly resistive crystalline phases.[1–3] It has many merits such as excellent endurance, non-destructive read, direct overwrite, low programming energy, huge read dynamic range, fast speed, high performance, good complementary metal–oxide–semiconductor (CMOS) logic compatibility, multi-state storage, and so on.[1]

As discussed by Lai, one of the biggest obstacles for production of PRAM is its high RESET current, for instance, typically higher than 1 mA based on 180 nm lithography.[1,3] Solutions to such a problem mainly include selection or change of chalcogenides based on material properties and structure optimization. Horii *et al.* and Matsuzaki *et al.* have developed PRAM cells with low RESET current by doping nitrogen and oxygen into $Ge_2Sb_2Te_2$ (GST), respectively.[4,5] Ha *et al.* reported an edge contact PRAM cell and Pellizzer *et al.* proposed a μ-trench architecture to reduce the RESET current.[6] Like conventional vertical normal bottom contact (NBC) PRAM cell, these structures also have a resistive heater of a high resistivity, which results in the requirement for high power consumption for phase change. In this letter, we will report a lateral PRAM cell without a resistive heater and demonstrate low power required for switching. High energy efficiency in such a cell is available in that the reversible phase change is attributed not mainly to the heat transfer from the resistive heater but mainly to self Joule heating of chalcogenide GST channel.

The cross-sectional diagram of the fabricated lateral PRAM device is schematically shown in Fig. 1. Such a device structure is adopted to investigate both phase change and field effect of chalcogenides. Only the former was studied at present and is reported here. SiN and SiO_2 under TiN electrodes are used for thermal isolation. The 200-nm-thick GST layer was deposited using a rf sputtering equipment (MNS-3000-RF, ULVAC, Inc.) at a background pressure below 5×10^{-5} Pa and a sputtering pressure of 0.2 Pa. The deposition rate of GST material was approximately 0.448 nm/s.[7] A 300-nm-thick capping layer of ZnS–SiO_2 was finally deposited to protect the GST channel from oxidation, thermal dissipation, and mechanical damage. The top-view scanning electron microscopy (SEM) image of a device is shown in Fig. 2. Specially, there is a confined GST channel connected by two wide TiN electrodes with a low resistivity in our lateral structure.

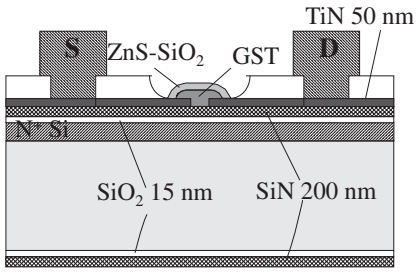

Fig. 1. Cross-sectional diagram of our fabricated lateral PRAM device with TiN electrodes of relatively low resistivity.

Current–voltage (I–V) characteristics of the device samples were measured by semiconductor parameter analyzer (4155B: Agilent Technologies, Ltd.). A waveform generator (Model 2571: Tabor Electronics Ltd.) was adopted to apply single pulses to devices.

Experiments for SET and RESET operations were performed in our lateral PRAM cells at first. As is well known, a low-resistance (LR) SET state would be obtained due to crystallization of chalcogenide by the application of a long and medium electrical SET pulse. On the other hand, a short and high electrical RESET pulse could induce a high-resistance (HR) RESET state due to amorphization of chalcogenide.[7–11] Pulse widths of 50 and 20 ns were used for SET and RESET operations in our experiments, respectively.

Figure 3(a) shows the typical experimental results for SET operation. The measurement began with a virgin as-deposited RESET state. Pulses with increasing pulse ampli-

*E-mail address: yinyou@el.gunma-u.ac.jp

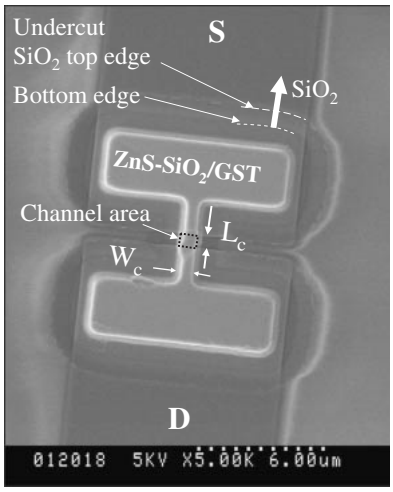

Fig. 2. Top-view SEM image of one of our as-fabricated lateral devices.

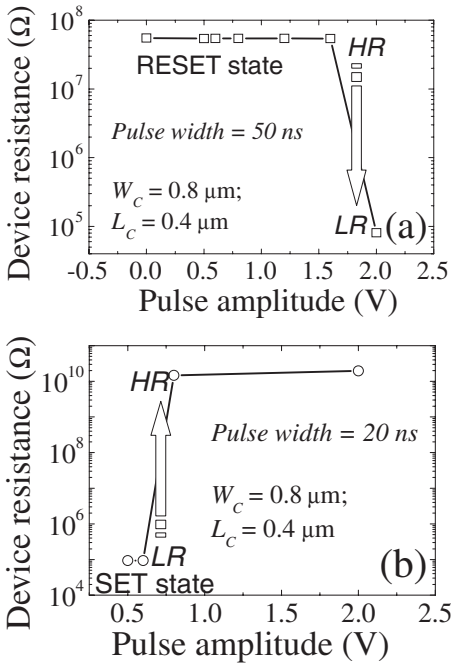

Fig. 3. Typical relationships between resistance and programming pulse amplitude of a single lateral PRAM sample for (a) SET operation and (b) RESET operation.

tudes were applied to a lateral device with a channel width W_C of 0.8 μm and a channel length L_C of 0.4 μm. Resistance was read at a low voltage after each of pulse application. The resistance of the as-deposited state device is approximately 6×10^7 Ω. However, the resistance was markedly decreased by approximately three orders of magnitude to 8×10^4 Ω after a pulse of 2 V was applied. The voltage pulse of 2 V here corresponds to approximately 40 nA in current value.

Figure 3(b) shows the typical experimental results for RESET operation. The measurement began with the above performed SET state. Pulses with increasing pulse amplitudes were applied to the above device. Resistance was also read after each of pulse application. The resistance was markedly increased after a pulse of 0.8 V was applied. The voltage pulse of 0.8 V here corresponds to approximately 10 μA.

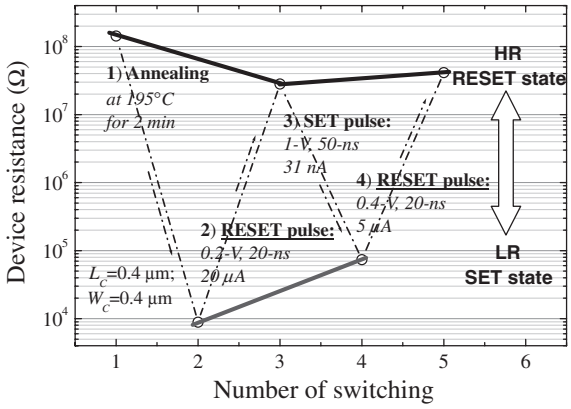

Fig. 4. Typical reversible switching between SET and RESET states in a lateral PRAM device.

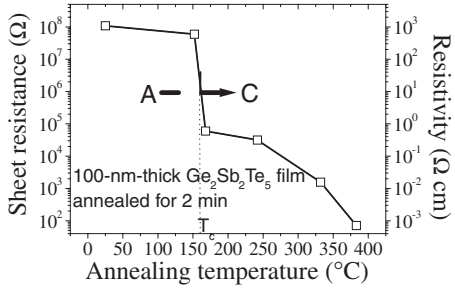

Fig. 5. Sheet resistance and resistivity of GST films as a function of annealing temperature. "A" represents amorphous, "C" represents crystalline.[7)]

A typical reversible switching between HR and LR states is shown in Fig. 4 using a device sample with a channel width of 0.4 μm and a channel length of 0.4 μm. The device sample was annealed at 195 °C for 2 min at first. A face-centered-cubic crystal structure would have been obtained in the chalcogenide GST film according to our experimental results.[7,8)] Device resistance correspondingly dropped approximately four orders of magnitude due to crystallization induced by isothermal annealing. Voltage pulse amplitudes as well as currents estimated on the basis of resistance and voltage of the applied pulses are shown for each of switching between LR and HR states. As we can see, the SET and RESET currents for switching operation could be as low as 30–40 nA and 5–20 μA, respectively. Operation currents and powers in the lateral structure could be one or two orders of magnitude lower than those of reported conventional PRAM. The power for SET and RESET operations is as low as approximately 0.03 and 3 μW, respectively. And it should be noted that the fast speed remained at such low operation currents and power consumptions.

The described resistive switching should result from structural transformation of GST between amorphous and crystalline phases. We fabricated the film samples at the same condition as the device samples. The resistivity of GST as a function of the annealing temperature is shown in Fig. 5. On the other hand, the roughly calculated resistivity of GST channel of the device used in Fig. 4 based on the channel dimension parameters is in the range from approximately 1 to approximately 10^3 Ω·cm. The

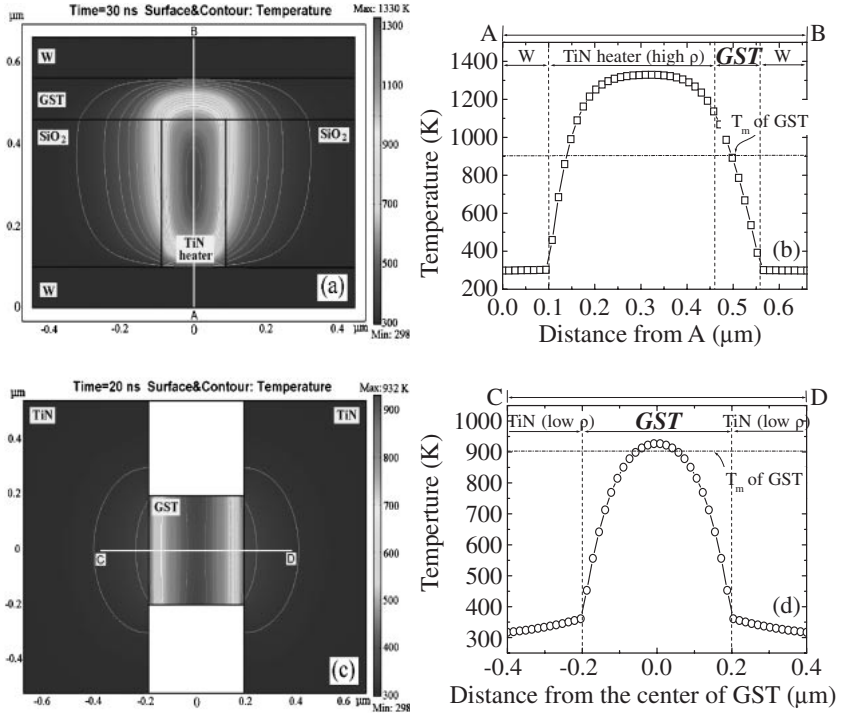

Fig. 6. (a) and (c) Simulated temperature distributions of conventional vertical PRAM cell with a resistive heater of a relatively high resistivity and our lateral PRAM cell with TiN electrodes of relatively low resistivity, respectively. (b) and (d) Temperature profiles along AB in (a) and CD in (c), respectively.

resistivity change is in the range of the amorphous–crystalline transition as shown in Fig. 5. Hence, the device reversible resistance change as shown in Fig. 4 is certainly due to structural switching between amorphous and crystalline phases.

Experiments as shown in Fig. 3 were conducted by using as-deposited devices, while we reversibly switched devices after annealing at a high temperature as shown in Fig. 4. The difference in resistance between in Figs. 3 and 4 results from different channel widths of the devices and possibly from dimension deviation due to lithography and lift off processes. Anyway, the resistance switching shown in Figs. 3 and 4 should be reasonably considered to be due to phase change between amorphous and crystalline from above analysis.

Next, let us compare simulation results on temperature distributions between a conventional NBC cell with a TiN resistive heater and our lateral cell with TiN electrodes of low resistivity when we amorphize these cells into their own RESET states. They are shown in Figs. 6(a) and 6(c), respectively. The detailed temperature profiles along the middle of the vertical and lateral cells are plotted in Figs. 6(b) and 6(d), respectively. It is well known that resistivity of TiN could be well controlled by adjusting its composition, impurity level, and film deposition condition.[12] In our simulation, the resistivities of the heater in NBC cell and the TiN electrodes of our lateral cell are taken to be $1.2 \times 10^{-4}\,\Omega\cdot m$[13] and $5 \times 10^{-6}\,\Omega\cdot m$ according to reported and our experimental results, respetively. The resistivity of GST is taken to be $0.8 \times 10^{-4}\,\Omega\cdot m$ in both of cells. It is clear that the temperature increase of GST in the NBC cell results mainly from thermal conduction from the TiN heater and scarcely from self heating of GST. On the contrary, in the lateral device without a heater, almost all of Joule heating occurs in GST and directly heat GST itself. As a consequence, PRAM with electrodes of a relatively low resistivity could have some advantages such as ultra low operation currents and power consumptions.

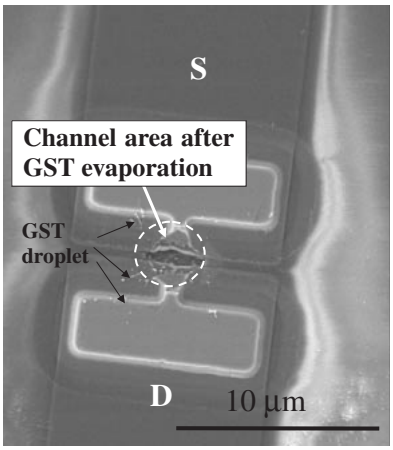

Fig. 7. Typical SEM image showing the failure due to evaporation of the GST channel.

The switching number for our current devices is small as shown in Fig. 4. Most of devices were stuck at a HR state after a few switching cycles. These devices after failure were analyzed by using SEM. A typical SEM image is shown in Fig. 7. The reason for the failure of our current devices is thought to be evaporation of the GST channel. The broken channel area and small droplets around it reveal that the GST channel was melted and then evaporated. Because of high thermal stress caused by rapid large temperature rise in the GST channel in the RESET operation, the weak regions of capping layer surrounding GST channel, for instance, sides of the channel might be broken and melted GST might be then given off. Little of it splashes around the GST channel and most of it evaporates into the air. After evaporation of the GST channel, the drain electrode will be cut off from the

source electrode. Consequently, a device after such a failure will be finally struck at a HR state.

By adopting a thick and large capping layer instead of a small one with the same size as the underlying GST layer, it would strongly suppress the thermal stress and thus protect melted GST from evaporation. Furthermore, a suitable resistor in series will be used for current limitation when we apply a pulse to the device for RESET operation. These two improvements are under investigation.

In summary, we investigated a lateral PRAM cell structure with a confined GST channel connected by two wide TiN electrodes of a relatively low resistivity. The RESET current and power consumption of the lateral cell are one or two orders lower than those of conventional bottom contact PRAM cell with a resistive heater, which results from high energy efficiency of utilization in heat generated by Joule heating in our lateral cell structure. Furthermore, the write/erase speed could be as fast as reported conventional vertical cell.

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